Power- and Reliability-Aware (Integrated) Design: Challenges and Opportunities

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Acknowledgements

- Victor Zyuban, IBM
- Alper Buyuktosunoglu, IBM
- Zhigang Hu, IBM
- Viji Srinivasan, IBM
- Hans Jacobson, IBM
- Jude Rivers, IBM
- Phil Emma, IBM
- Hendrik Hamann, IBM
- Jaime Moreno, IBM
- Plus, many others at IBM
  - including interns/coops

- Sarita Adve, U of Illinois
- Kevin Skadron, U of Virginia
- Margaret Martonosi, Princeton Univ.
- David Albonesi, Cornell University
- … and some of their students

Disclaimer:
The views and opinions expressed in this talk are the speaker’s own, and do not reflect any real IBM product plans or trends.
Talk Outline

A. Technology trends: why are power and reliability important now?
   - Power, pwr-density, temp, perf, reliability: multi-dimensional optimization problem
     - The need for appropriate metrics for early-stage design trade-offs
   - Integrated microarchitectures: what and why?

B. Power-aware microarchitectures: key advances in the last five years
   - Microarchitecture-level integrated simulators; validation/calibration
   - Key techniques of promise in real design; potential pitfalls
   - Chip-level microarchitecture trends (governed by the power problem)

C. Reliability-aware microarchitectures: past approaches vs. new ones
   - Modeling support for hard and soft error analysis at microarch level
   - Area-efficient error-tolerance support: new approaches of promise

D. Closing thoughts:
   - Towards integrated on-chip controllers
   - SoC-type designs for server processors?
Part A of Talk: about 20 mins
Technology Trends ➔ Broad Architectural Implications
Moore’s Law Continues

Heading toward 1 billion transistors in 2007

330 million transistors on 90 nm SRAM

(as reported in ISSCC-03)

Courtesy: S. Tyagi, Intel

Note also: increasing transistor count => potentially increasing chip-level failure rate!
(But)...Power is Limiting CMOS Microprocessor Frequencies

Server microprocessors cannot simultaneously utilize all their transistors due to power limitations

- Moore’s law is continuing with respect to transistor density, although at a reduced pace
- Workload demands are highly variable
- New methods to utilize silicon density scaling will be developed to accommodate diverse workloads while managing power constraints

S. Kosonocky, IBM; presentation at Univ. of Michigan, 2004
Module Heat Flux Trend

- Year of Announcement
- Module Heat Flux: (watts/cm²)

Bipolar

- IBM ES9000
- CMOS
- Latest high-end processors (Intel and IBM)
- Fujitsu VP2000
- IBM 3090S
- NTT
- Fujitsu M-780
- IBM 3090

Start of Water Cooling

- Vacuum
- IBM 360
- IBM 370
- IBM 3033
- Fujitsu M380
- IBM 3033
- CDC Cyber 205
- IBM 4381
- IBM 3081

Latest high-end processors:
- IBM P4 (initial)
- IBM P4
- IBM RY5
- IBM RY7
- IBM RY6
- Pentium 4
- Pulsar
- Apache
- Merced
- Pentium II (DSIP)
Power-performance efficiency: choice of metric matters!

Data source: Berkeley CPU Center and http://www.specbench.org; and other single processor-level data (estimated)

What's the right metric to use in early-stage power-perf tradeoff analysis in microarch. research?
Power Consumption vs. Cooling Cost

S. H. Gunther et al., Intel Technology Journal, 2001

By the way: a more appropriate x-axis metric to plot would be:

watts/sq.mm per degree Kelvin above ambient
Power-Aware vs. Temperature-Aware

Test case: chip 18 x 12 mm\(^2\) in a standard cooling package....

<table>
<thead>
<tr>
<th>Power-aware design</th>
<th>Temperature-aware design</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{\text{total}} = 25\ W)</td>
<td>(P_{\text{total}} = 100\ W)</td>
</tr>
<tr>
<td>Power map</td>
<td>Power map</td>
</tr>
<tr>
<td>185 W/cm(^2)</td>
<td>46 W/cm(^2)</td>
</tr>
<tr>
<td>0 W/cm(^2)</td>
<td>12 W/cm(^2)</td>
</tr>
<tr>
<td>93 K</td>
<td>41 K</td>
</tr>
</tbody>
</table>

save 10 W in low power density region (\(P_{\text{total}}=40W\))

| Power map | Temp map |
| 185 W/cm\(^2\) | 96 K |
| 12 W/cm\(^2\) | |

save 10 W in high power density region (\(P_{\text{total}}=40W\))

| Power map | Temp map |
| 111 W/cm\(^2\) | 61 K |
| 21 W/cm\(^2\) | |

Courtesy: Hendrik Hamann, Thermal Physics Dept., IBM Research
Dimensional Variability: The Latest Limiter

- The critical dimensions in our designs are scaling faster than our control over them.

- Chip robustness with respect to manufacturing and environmental variations is as important as speed and power.

- Implications:
  - Design for worst case
  - Use chip area to get performance
  - Design reliable system with unreliable components
  - GALS/MCD microarchs?
  - On-chip microcontroller?

Albonesi et al. (Cornell), Marculesu et al. (CMU), …

Other asynch. arch. research at Cornell and elsewhere
Variability Affects Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Delay Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEOL metal (metal mistrack, thin/thick wires)</td>
<td>-10% to +25%</td>
</tr>
<tr>
<td>Environmental (voltage islands, IR drop, temperature)</td>
<td>±15 %</td>
</tr>
<tr>
<td>Device fatigue (NBTI, Hot Electrons)</td>
<td>±10%</td>
</tr>
<tr>
<td>Low threshold voltage ($V_t$) tracking (up to 8 device families in cu08)</td>
<td>± 5%</td>
</tr>
<tr>
<td>Model/hardware uncertainty (per cell type)</td>
<td>± 5%</td>
</tr>
<tr>
<td>N/P mistrack (fast rise/slow fall, fast fall/slow rise)</td>
<td>±10%</td>
</tr>
<tr>
<td>PLL (jitter, duty cycle, phase error)</td>
<td>±10%</td>
</tr>
</tbody>
</table>

- Requires [-55%, +80%] guard band
Variability Affects Functionality (Reliability)

- SRAMs use minimum-sized devices and are affected the most by intra-die variations in device dimensions and threshold voltage.
- Variations result in mismatch of device strengths and can render read operations unstable (i.e., they flip the value stored in the cell)
  - Affects correct operation of SRAMs
  - Poses challenge for scaling of 6T SRAM cells
Soft Error Rate Escalation: *the other consequence of scaling*

**Latch Qcrit and alpha SER**

![Graph showing Latch Qcrit and alpha SER](image)

**Projected Trends in SER**

![Graph showing Projected Trends in SER](image)

*Figure 14. SER/chip for SRAM/latches/logic*

Shivakumar et al. DSN-2002
Impact of Scaling on FIT rate

- Total FIT (failures in time) rate increases with scaling: 316% on average
- Large range among applications: 104% of average at 65nm
- Worst-case much higher: most conservatively, 90% higher

Caveat: hypothetical study of blindly scaling a POWER4-like processor, without any design tweaks
Accommodating technology uncertainty

- **Chip-level functional robustness declining in future technologies**
  - increase in transient and permanent errors:
    - power density and temperature problems (hot spots) is an example factor
    - Ldi/dt noise (exacerbated by dynamic power management) – another example
    - Full chip burn-in limited by leakage power
    - Soft error rates on the rise due to technology factors
  - Power, area, yield (cost) pressures ➔ less scope for redundancy thru’ replication
  - increase in chip complexity ➔ impacts verification time (cost)
  - Technological uncertainties in the DSM (deep sub-micron) era will impact design and CAD tools at all levels of abstraction

What are the right joint metrics to use in early-stage trade-off analysis?

We may be entering a disruptive period where tradeoffs between single-chip performance, power and reliability become mandatory
Power- and reliability-awareness at the highest levels of design abstraction

- **(Micro)-Architecture & Compilers**
  - Optimize basic pipeline depth for power-perf-reliability
    - Optimize number of cores per die
    - Optimize core complexity and threading
  - Shrink structures; reduce complexity
  - Shorten wires; link early definition to floorplan
  - Reduce activity factors:
    - gate clock, Ifetch, …
    - adapt resource sizes
  - Turn on units on-demand; gate $V_{dd}$ (predictive)
  - Trade off parallelism against clock frequency
  - Reduce wasted work: “standard” operations

- **Operating Systems**
  - Natural: OS is traditional resource manager
  - Equal energy scheduling
  - Thermally-aware adaptation

- **Application/Algorithm**
  - Additional opportunities; open research issues..
Broad Implication: *Integrated* Microarchitectures

- Frequency growth curb has led to the trend of lower frequency, multi-core chip microarchitectures
  - recent announcements by Intel and Sun consolidate industry-wide trend

- Technological trends coupled with design trends dictated by power-awareness is leading to the prospect of degraded chip-level reliability and/or reduced performance growth even after the “right hand turn” to lower frequency, multi-core designs
  - unused cores or sub-cores must be power-gated off, depending on workload demand, to save power, perhaps at some performance cost
  - temperature-aware floorplan and dynamic activity migration will be needed to mitigate hot spot problems, again at some performance cost
  - on-chip power and temperature management must be balanced against performance and reliability budgets; error tolerance must be done at low cost (area overhead)
  - intra- and inter-chip variability will require variation-tolerant design, one that adapts to chip-specific operating frequency and thermal design point on “power-on” and perhaps dynamically

- multi-dimensional optimization and continuous self-calibration → will require integrated, on-chip controller that manages multiple, possibly heterogeneous computing cores and storage resources
  - area pressure (leakage, yield) will force such multi-dimensional optimizers (controllers) to be hardware-software solutions (i.e. will involve the compiler, hypervisor, OS)
  - server processor chips will increasingly become SoC like
Part B of Talk: about 15 mins
Power-Aware Microarchitectures:  
Key Advances in Design and Modeling
Server Chip: Unconstrained Power

Pre-silicon, POWER4-like superscalar design

D. Brooks, et. al. MICRO-03 (tutorial)
New generation, integrated modeling infrastructure


Power Modeling Enhancements → Package RLC models, Ldi/dt analysis

PowerTimer: core-level modeling

Temperature Modeling → Reliability Modeling

VALIDATION

Substrate simulator: Turandot

Latch-counts + array power models
Latch-counts + scaled CPAM based models + refined array power models
Trace/exec driven simulation

U of Virginia’s
HotSpot,
later modified

System interconnect and tech. scaling parameters, models
Uniprocessor CPI and Power sensitivities

Multi-Core Power-Performance Modeling

chip-level microarchitecture modeling

microarch design and definition

Data from device and circuit level
Program traces

Cycle acc. Processor Simulator
Soft error model
Architectural derating factor

To Interconnect
Layer Thermal Model
Heat Sink
Heat Spreader
Thermal Interface Material
Fin-to-air convection thermal resister

L2
C7
L2
C0
L2
C4
L2
C8

Trace/exec driven simulation
Typical CMP Thermal Map [PowerTimer/Turandot]
Overall Validation Methodology (PowerTimer)

- **PowerTimer**
  - Next test case
  - Timeline output
- **Reference Model** (e.g. M2 or M3)
- **LaSpecs**
  - Tabular (html) web specs
  - Detect mismatch
- **Temperature Model**
  - Simulated chip temp profile
- **Comparison**
  - Direct image of chip temp profile

- **Detect anomalies**
- **Detect mismatch**
- **CPI and utilization bounds**
- **CPI and utilization stats**
- **Elpaso bounds timer**

(ongoing work)

H. Hamann, et al.
Thinned processor chip during bootup

~ 100 W/cm² @ 3.4 GHz
peak temperatures of ~ 80°C
base temperature 20°C

Very localized hot spots in different locations

Courtesy, Hendrik Hamann
Thermal Physics, IBM

(movie: will not show on pdf version of slideset; sorry!)
Clock-gating: the modern baseline power-saver

- Conventional clock-gating summary
  - **Effective, low-complexity, low-overhead scheme for reduction of active power in microprocessors**
    - was already prevalent in embedded processors and ASICs
    - now the main power management technique in server-class processors
    - 20 to 50% reduction in active power, depending on workload and granularity of gating
    - temperature reduction leads to leakage power savings as well

- New advances in clock-gating stretch the limit of gating efficiency
  - Transparent latch clock-gating
  - Elastic pipeline clock-gating
    (H. Jacobson et al., ISLPED-04, ASYNC-02, HPCA-05)
Clock-gating helps reduce leakage power as well!

POWER5 Chip

w/o CG  with CG

Thermal Image Plots (measured)
Transparent Clock-Gating: Basic Idea

- **Traditional opaque-mode clock gating is not optimal**
  - Generates significant amount of clock pulses that are redundant to the correct operation of the pipeline
  - Problem is that latches are held opaque by default (when gated off)
  - Requires every latch to be clocked in order to pass a data item through the pipeline

- **Idea: hold latches in the transparent mode by default (when gated off)**
  - Data items can pass through pipeline without clocking if they are sufficiently spaced in time
  - Latches are only clocked when needed to avoid data races for closely spaced data items
  - Called “Transparent Clock Gating”

- **Transparent gating allows gating clock to active pipeline stages**

H. Jacobson, ISLPED-04
Clock Power Reduction via Transparent CG

H. Jacobson, P. Bose et al., HPCA-2005
Potential Compound Effect

- **Compound effect vs. traditional techniques (FPU)**
  - Total clock power reduction of 66%
    - Elastic stall clock gating (5%)
    - Register level clock gating (25%)
    - Transparent clock gating (36%)

H. Jacobson, P. Bose et al., HPCA-2005
Power-Performance Efficient Processor Core
Pipelines: *definition and analysis*
Deducing Optimal Pipe Depths

V. Srinivasan et al., MICRO-35, 2002
V. Zyuban et al., IEEETC, 8/2004

Power-performance optimal
Performance optimal

Relative to Optimal FO4

SPEC2000 suite
Workload impact: TPCC Trace

Power-performance optimal

Performance optimal

Relative to Optimal FO4

0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

0
10
20
30
40
50
60
70
80
90
100

Total FO4 Per Stage

bips
bips^3/W

is this the right metric?
what is the effect of leakage pwr?
what's the right joint metric for power-performance-reliability?
Some observations

- **Active power grows approximately as a square of the pipeline depth**
  - Superlinear growth in the number of latches
  - Linear growth in frequency

- **Leakage power grows sublinearly with the pipeline depth**
  - Growth in latch area
  - Growth in logic area
  - Growth in buffer sizes

- **In a leakage dominated design it is less prohibitive to go to deeper pipelines**
Impact on Design

Tradeoff via pipeline depth
Tradeoff via changing Vdd
Tradeoff via frequency

Maximum Power Budget

Optimal BIPS^3/W

Zyuban, et. al., Transactions on Computer' 04
Integrating Multiple Cores on Chip

- With uniprocessor performance improvements slowing, multiple cores/threads per chip/socket will help continue the exponential system performance growth
- Exploit performance through higher levels of integration in chips, modules, and systems
- Invest power in chip-level performance rather than core performance

POWER 4: 2001
180 nm, Cu, SOI
2 cores / chip

POWER 4+: 130 nm

POWER 5: 2004
130 nm, Cu, SOI
2 cores / chip
2 way SMT / core
Building Blocks for Chip-level Integration

For a given power budget, higher throughput is achieved by multiple simple cores on both SMP workloads and independent threads.

The appropriate design point depends on the workload that is being supported. Scaling up a simple core by reducing FO4 and/or raising Vdd does not achieve this level of performance.

It may be worthwhile to have multiple heterogeneous cores on chip.

Source: Zyuban et al. IBM tech. report 2004
In homogeneous design: number and complexity of cores must be determined

In heterogeneous design: core- or sub-core-level power gating support must be worked out

One approach to balanced single-thread and chip throughput performance: lots of simple cores that can be organized to exploit single-thread ILP in (possibly speculative) multi-threaded mode

- Lots of power-efficiency issues in such ILP/TLP reconfigurable architectures
SMT Power Efficiency

- SMT is a power-efficient design paradigm for modern, superscalar microarchitectures
  - performance gains of nearly 20% with a power uplift of roughly 24% leading to significant reduction in $ED^2$ [Turandot/PowerTimer results]
  - actual POWER5 simulation and measurement data shows significantly higher chip IPC gains for commercial workloads (40-60%) gain, with about 15-20% power uplift, 20% area overhead

Peak Temperature: SMT vs. CMP

3 heat-up mechanisms

- **Unit self heating** determined by the power density of the unit
- **Lateral thermal coupling** between neighboring units
- **Global heating** through TIM (thermal interface material), heat spreader, and heat sink

This result is controversial, needs to be validated!

Y. Li, Z. Hu et al., P=AC², 2004
Conclusions about temp. efficiency (SMT, CMP)

For POWER4/5-like architecture,

- CMP and SMT temperatures are comparable with current generation process technologies, but their thermal heating mechanisms are quite different.
  - SMT heating is primarily caused by localized heating within certain key micro-architectural structures such as the register file, due to increased utilization.
  - CMP heating is primarily caused by the global impact of increased energy output.

- When leakage power is significant, CMP machines are clearly hotter than SMT.

- With the same chip area, SMT performs better than CMP for memory bound benchmarks while CMP wins for non-memory bound workload.

- Localized DTM schemes perform better for SMT while global DTM schemes favor CMP.

Y. Li, Z. Hu et al., P=AC², 2004
Predictive Power Gating
Virtual Vdd discharge in the power gated mode
Key Intervals in the Power Gating Cycle

\[ T_{\text{break even}} \sim 10-17 \text{ cycles} \]

- Voltage at virtual Vdd
- Saved energy per cycle
- Aggregate saved energy
- Overhead energy

Z. Hu, et. al., ISLPED’04
Power Gating Potential: Example

FPU, FXU gating potential for different values of $T_{\text{break-even}}$ running SPECfp2K benchmarks

Z. Hu, et. al., ISLPED’04
Time-Based Power Gating Results: Example

for FPU running SPECfp2K benchmarks

Z. Hu, et. al., ISLPED’04
Adaptive Microarchitectures

Joint work with D. Albonesi (U of Rochester/Cornell)
J. Smith (Wisconsin)
Exploiting Workload Variability: On-Demand Reconfiguration

- Adapt queue/buffer sizes or cache configuration on-demand, to save power (ISLPED-02)
- Adapt instruction fetch/dispatch rates (fetch gating, ISLPED-02 ISCA-03)
- Adapt clock speeds or voltages dynamically
  - ✓ Detect/predict phases and their duration

Example High-End Processor: TPC-C workload

Trace interval size = 0.5 million instructions

Interval Number

CPI

Inst. Buffer Size
- 64
- 56
- 48
- 40
- 32
- 24

CPI

1.8
2
2.2
2.4
2.6
2.8
3
3.2
Power-Aware Microarchitecture: summary

- **Power-perf efficient choice of initial pipeline depth (FO4 per stage)**
  - A fundamental error here could lead to post-silicon power-performance (and hence, cost-performance) deficiency

- **Area and leakage-efficient design**
  - Simpler cores; balanced single- vs. multi-thread performance
  - Fine-grain power-gated to further reduce leakage
    - Predictive support built into microarchitecture & compiler to minimize overhead

- **Gated clock, bandwidth (fetch, issue, …), register ports …**
  - Granularity of application determines active power savings
  - Cycle-time pressure may inhibit pervasive gating throughout the logic
    - Verification complexity is another concern

- **Adaptive (reconfigurable, resizable) resources**
  - Applicable to on-chip logic *and* buffers (caches, registers, etc)
  - Potentially save active *and* leakage power
  - Workload phase detection and prediction are key elements of adaptive design
Part C of Talk: about 10 mins

Reliability-Aware Microarchitectures:  
Design and Modeling
Reliability-aware microarchitecture research at IBM: progress so far

- **RAMP**: Reliability Aware MicroProcessor Design [ISCA’04]
  Architecture-level model for lifetime reliability analysis
  Uses state-of-the-art device level models for wear-out failures

- **Scaling analysis** on POWER4-like core [DSN’04]
  Quantified impact of scaling on lifetime reliability

- **Dynamic Reliability Management** [ISCA’04]
  Architectural technique for reliability control

- **Exploiting Structural Duplication for Lifetime Reliability** [ISCA’05]
  Performance-area-reliability tradeoffs with selective duplication

- **SoftArch**: microarchitecture-level MTTF projection for given incident soft error rates [DSN’05]

Collaborative Work with Sarita Adve’s Group at UIUC
Hard Fail Rates: contributions from individual effects

EM and TDDB of most concern (temperature and scaling effects)

SM and TC seem more manageable (temperature only)

Actually, NBTI is the most worrisome new effect

J. Srinivasan et al., DSN-04
DRM (dynamic reliability management) potential

400 K - Current reliability qualification, overdesigned (lower bound)
370 K - Application based reliability qualification
345 K - Qualification for average application
325 K - Underdesigned for reliability

J. Srinivasan et al. ISCA-04
Cost/Performance Tradeoff Analysis for Designs with Built-in Redundancy

For limited overheads, GPD more beneficial
For larger overheads, SD or SD+GPD more beneficial

J. Srinivasan et al. ISCA-05
Adaptive (Autonomic) Control to Maintain Safe Margins

- Ongoing research: practically feasible on-chip adaptive control to ensure reliable operation

- Microarchitectural prediction techniques used effectively to anticipate workload phases and events - i.e. periods of activity, inactivity and specific noise (Ldi/dt) events
  - preliminary workload characterization studies have yielded encouraging results
  - predictive feature helps minimize performance overheads

Illustrative example (not real experimental data)

**SoftArch: IBM’s architecture-level SER analysis methodology**

System SER rate, FIT, MTBF

Workload traces

Bit-fail cross sections for SRAM cells

Neutron flux

SEM1M simulator

Technology parameters

Ckt simulator Qcrit

Ckt Level Simulator

Current pulses

Logic error rate

X. Li et al., DSN-05

X. Li, J. Rivers, P. Bose, R. Puri (in collaboration with Sarita Adve)
Results – Architectural FIT rate

Results obtained are similar to AVF methodology (Shubu Mukherjee, et al., Intel)

- Significant architectural masking (79% int, 87% fp)
- Variations across workload
  - Different utilizations for different workloads
Intel Data on Architectural Derating Effect

Dynamic Instr. Breakdown

- DYNAMICALLY DEAD: 20%
- PERFORMANCE INST: 1%
- PREDICATED FALSE: 7%
- NOP: 26%
- ACE: 46%

Average across Spec2K

Instruction Queue

- IDLE: 31%
- ACE: 29%
- NOP: 15%
- Ex-ACE: 10%
- DYNAMICALLY DEAD: 8%
- PERFORMANCE INST: 1%
- WRONG PATH: 3%
- PREDICATED FALSE: 3%

ACE: architecturally correct execution, Contributing to AVF: arch. Vulnerability Factor; e.g. AVF = 0% for branch predictor array; = 100% for PC

Shubu Mukherjee et al., HPCA-2005
But… the “metrics” issue persists!

\[ \text{MTTF} = \frac{1}{(\sum_{i} \lambda_i)} \]

\[ R_i(t) = e^{-\lambda_i t} \]

\[ \lambda_i = \text{failure rate of ith component in the system, usually measured in units of FITs} \]

Q. This method of projecting mean time to failure for a system: is this good enough (in all scenarios), or is there a need for change?
And, is MTTF the right reliability metric in all scenarios anyway?

Better MTTF, but much larger variance!!
Part D of Talk: about 5 mins

Concluding Thoughts
Integrated, SoC-like Server-Class Microarchitectures

- Multi-core processors will need complex, on-chip management to maintain balance between power, temperature, reliability and performance
  - Adjusting dynamically to temperature-sensitive variabilities will also be required
  - Field BIST may augment pre-silicon verification
  - Graceful, managed degradation and/or managed replacement/sparing may be needed to extend chip lifetime or control degree of soft error tolerance
  - Managing redundant resources for dynamic reliability-performance tradeoffs
  - Intel’s Montecito (Foxton controller) may be a trend-setter in this regard

- Integrated hardware-software solutions to minimize hardware complexity and added power, are likely

- Server-class processor chip designs are likely to resemble SoC-like architectures with attended design methodologies in future
  - Power-efficient “scale-out” servers (a la Blue Gene)
  - Cost-effective RAS solution via h/w-s/w integrated design

Integrated pre-silicon modeling challenges!
Hardware Integration in BlueGene/L: System-on-a-Chip ASIC

- IBM CU-11, 0.13 µm
- 11 x 11 mm die size
- 25 x 32 mm CBGA
- 474 pins, 328 signal
- 1.5/2.5 Volt

Integrated functionality
- Two PPC 440 cores
- Two “double FPUs”
- L2 and L3 caches
- Torus network
- Tree network
- JTAG
- Performance counters
- EDRAM
Thank you!